PATENT
02-ZAV-221

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	: Group Art Unit: 2681
Jan Frans Lucien CRANINCKX	: Confirmation No.: 8145
Serial No.: 10/718,256	:
Filed: November 20, 2003	:
For: LOW FREQUENCY SELF-CALIBRATION OF A PLL WITH MULTIPHASE CLOCKS	:

CLAIM FOR PRIORITY UNDER 35 U.S.C. §119

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Under the provisions of 35 U.S.C. §119, there is filed herewith a certified copy of European Application No. 02447228.4, filed November 21, 2002, in accordance with the International Convention for the Protection of Industrial Property, 53 Stat. 1748, under which Applicant hereby claim priority.

Respectfully submitted,

Date: 5/21/04

By: _____
Stephen Bongini
Reg. No. 40,917

FLEIT, KAIN, GIBBONS,
GUTMAN, BONGINI & BIANCO P.L.
551 NW 77th Street, Suite 111
Boca Raton, Florida 33487
Telephone: (561) 989-9811
Facsimile: (561) 989-9812

Europäisches Patentamt	European Patent Office	Office européen des brevets

Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

02447228.4

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

ABSTRACT

LOW FREQUENCY SELF-CALIBRATION OF A PLL WITH MULTIPHASE CLOCKS

A Phase-Locked Loop with multiphase clocks with

- a main loop comprising a Phase Frequency Detector (1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (4) and a Phase-switching Fractional Divider (5), coupled in series,
- a calibration loop comprising a Calibration Charge Pump (6), a multiplexer (7) and Y Calibration Loop Filters (8), with Y being an integer,
- a Control Logic (9) arranged to control said Phase-Switching Fractional Divider (5) and said multiplexer (7), and
- a Reference Frequency Signal (10) applied to said Phase Frequency Detector (PFD)(1) and a calibration signal (11) applied to said calibration loop,

characterised in that the main loop comprises a Phase-adjusting block (12) coupled with a demultiplexer (13), wherein said Phase-adjusting block is arranged to receive correction signals from said calibration loop and said multiplexer is controlled by said Control Logic (9)

(Figure 2)

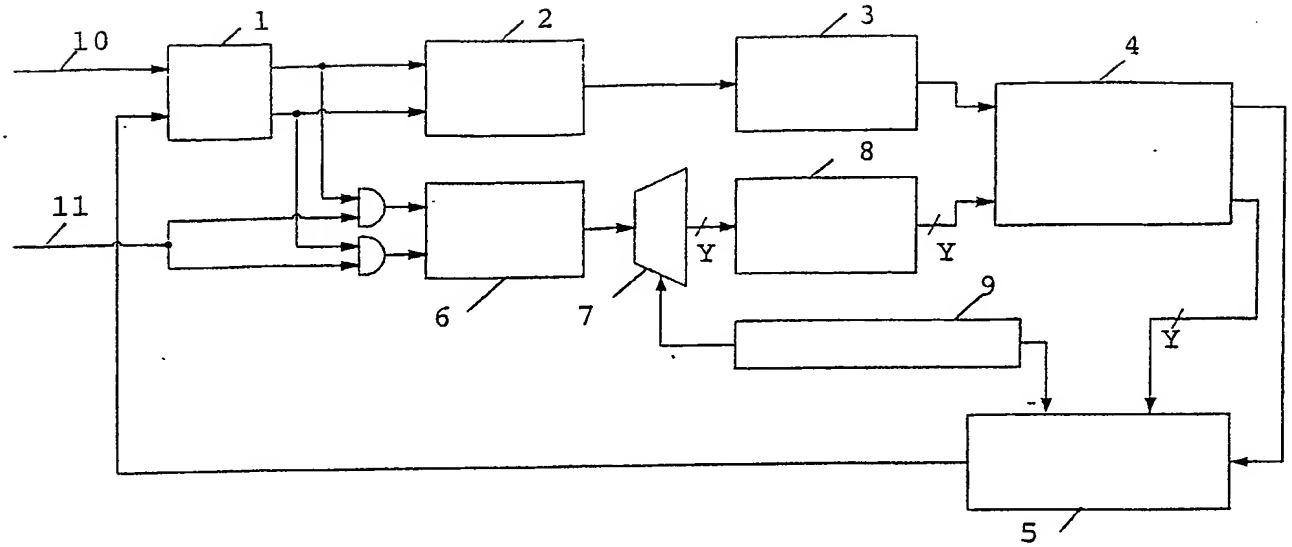

FIG. 1

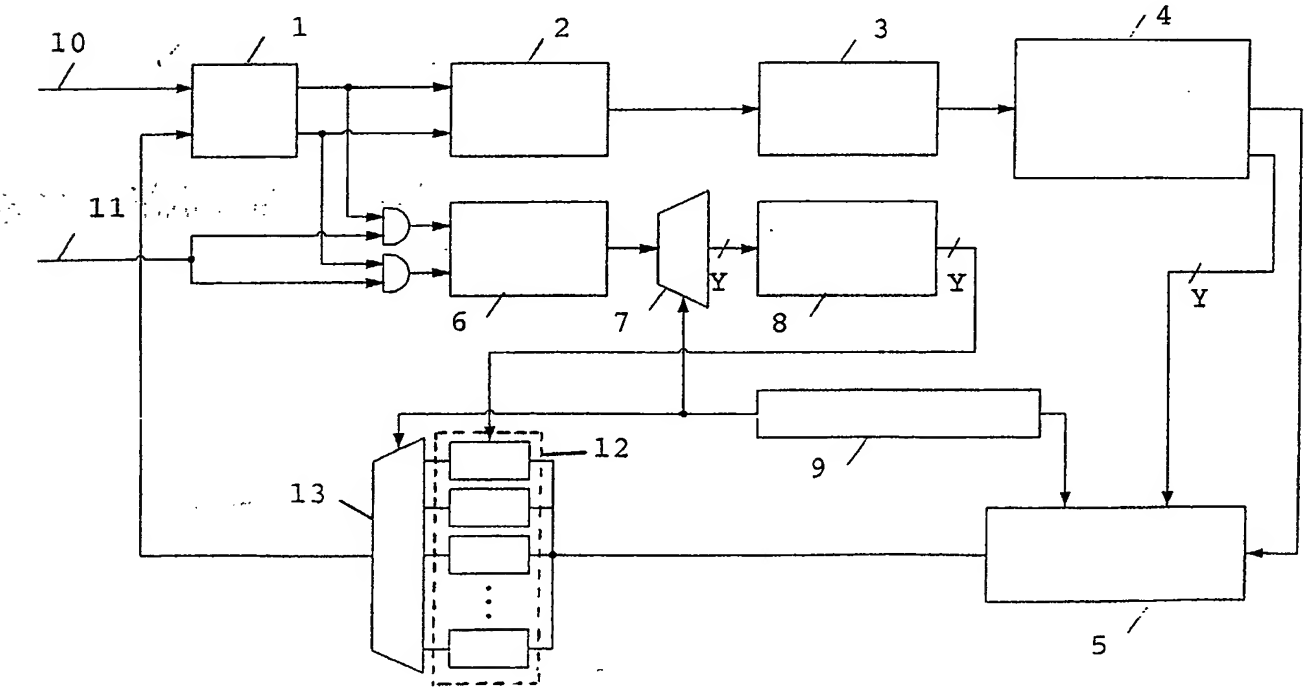

FIG. 2

CLAIMS

1. A Phase-Locked Loop with multiphase clocks with

- a main loop comprising a Phase Frequency Detector (1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (4) and a Phase-switching Fractional Divider (5), coupled in series,
- a calibration loop coupled to said a Phase Frequency Detector (1) and comprising a Calibration Charge Pump (6), a multiplexer (7) and Y Calibration Loop Filters (8), with Y being an integer,
- a Control Logic (9) arranged to control said Phase-Switching Fractional Divider (5) and said multiplexer (7), and
- a Reference Frequency Signal (10) applied to said Phase Frequency Detector (PFD)(1) and a calibration signal (11) applied to said calibration loop,

characterised in that the main loop comprises a Phase-adjusting block (12) coupled with a demultiplexer (13), wherein said Phase-adjusting block is arranged to receive correction signals from said calibration loop and said multiplexer (7) is controlled by said Control Logic (9),

2. A Phase-Locked Loop with multiphase clocks according to claim 1, **characterised in that** said Phase adjusting block (12) comprises Y low-frequency delay cells, Y being an integer, controlled by said Y calibration Loop Filters(8).

contained in the low-frequency delay cell corresponding to said phase.

4. A method for synthesizing frequencies with a Phase-Locked Loop with multiphase clocks, comprising the following steps :

- Providing a Phase-Locked Loop such as in claim 1
- Applying a reference frequency signal (10) to the Phase Frequency Detector (1) of the Phase-Locked Loop, and
- Applying a Calibration Signal (11) to the calibration loop (8) of the Phase-Locked Loop,

5. A fractional-N frequency synthesizer comprising a PLL as in claim 1 or implementing the method of claim 2.

6. An integrated circuit comprising a Phase-Locked Loop as in claim 1.

7. A digital mobile radio communication apparatus comprising a Phase-Locked Loop as as in claim 1 or implementing the method of claim 2.

(Main) loop comprises, coupled in cascade, a Phase Frequency Detector (PFD)(1), a Main Charge Pump (2), a Main Loop Filter (3), a Multi-Phase Voltage Controlled Oscillator (VCO)(4) and a Phase-switching Fractional Divider (5). A second loop (Calibration) comprises the series connection of a Calibration Charge Pump (6), a Multiplexer (7) and Y Calibration Loop Filters (8), with Y being an integer, coupled between said Phase Frequency Detector (PFD)(1) and said Multi-Phase Voltage Controlled Oscillator (VCO)(4). The Multiplexer (7) is controlled by a Control Logic (9) coupled to the Phase-Switching Fractional Divider (5). A Reference Frequency Signal (10) is being applied to said Phase Frequency Detector (1). The Calibration signal (11) is applied to a control input of the Control Logic (9).

[0018] Fig. 2 shows the block scheme of the invention. The Main Loop (1 to 5) remains the same. The second loop (Calibration) still comprises the series connection of a Calibration Charge Pump (6), a Multiplexer (7) and Y Calibration Loop Filters (8), with Y being an integer. The input still comes from the Phase Frequency Detector (PFD)(1), but the output is not connected anymore to said Multi-Phase Voltage Controlled Oscillator (VCO) but to a block (12) positioned after the Phase-Switching Fractional Divider, i.e. at lower frequency. Block (12) is the phase-adjusting block. As in the prior art (Fig.1) the Control Logic (9) must select the correct loop filter [1:Y] of the phase to be calibrated, based on the state the Phase-Switching Fractional Divider (5) is in. This is done with the multiplexer following the calibration charge pump (6). Additionally, the same control logic (9) must also select in (12) the corresponding low-frequency delay cell $\Delta T[1:Y]$ that is associated to this phase. This is done with

the de-multiplexer (13) shown in the block diagram.

[0019] The multi-phase VCO (4) can now be "non-calibratable" : the calibration loop now doesn't adjust the phases of the VCO directly, but instead adjusts the amount of delay given by the low-frequency delay cells $\Delta T[1:Y]$. If phase[i] of the VCO has an error of $\Delta\varphi[i]$ with respect to the ideal (matched) phase it should have, this is compensated by an equivalent delay (of the opposite sign) in the low-frequency delay cell. Because of this the phases at the input of the phase detector are mismatch-free and thus perfectly aligned. The fractional spurs in the output spectrum are thereby removed.

[0020] The PLL described above can advantageously be applied in a fractional-N frequency synthesizer.

these circuits, resulting in lower maximum operating frequency and/or higher power consumption.

Aims of the invention

[0005] The present invention aims to propose a product that synthesises a fractional-N frequency based on a Phase Locked Loop (PLL) with multiphase clocks, in which a self-calibrating loop is used in such a way that the fractional spurs problem is overcome.

Summary of the invention

[0006] The present invention is related to a Phase-Locked Loop with multiphase clocks with

- a main loop comprising a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider, coupled in series,
- a calibration loop comprising a Calibration Charge Pump, a Multiplexer and Y Calibration Loop Filters, with Y being an integer,
- a Control Logic arranged to control said Phase-Switching Fractional Divider and said multiplexer, and
- a Reference Frequency Signal applied to said Phase Frequency Detector and a calibration signal applied to said calibration loop.

[0007] Said main loop comprises a Phase-adjusting block coupled with a demultiplexer , wherein said Phase-adjusting block is arranged to receive correction signals from said calibration loop and said multiplexer is controlled by said Control Logic.

[0008] According to a preferred embodiment of the invention, said Phase adjusting block comprises Y low-

frequency delay cells, Y being an integer, controlled by said Y calibration Loop Filters.

[0009] According to a more specific embodiment the correction signal is a delay, specific to a phase, and is contained in the low-frequency delay cell corresponding to said phase.

[0010] As a second object the present invention is related to a method for synthesizing frequencies with a Phase-Locked Loop with multiphase clocks.

[0011] According to a preferred embodiment of the invention, the PLL is part of a fractional-N frequency synthesizer.

[0012] Advantageously, the Phase-Locked Loop is comprised in an integrated circuit.

[0013] In another preferred embodiment the Phase-Locked loop is comprised in a digital mobile radio communication apparatus.

Short description of the drawings

[0014] Fig. 1 represents the prior art solution.

[0015] Fig. 2 represents the invention.

Detailed description of the invention

[0016] The present invention relates to a Phase-Locked Loop (PLL) with multiphase clocks, in which a self-calibrating loop is used. If one just wants to solve the problem of the fractional spurs, the extra circuitry to adjust the phase of the multiphase clocks can advantageously be moved to the low frequency domain at the output of the phase-switching fractional divider. The calibration then is done with low-frequency blocks, resulting in higher maximum operating speed and/or lower power consumption.

[0017] Fig. 1 shows the prior art solution. A first

LOW FREQUENCY SELF-CALIBRATION OF A PLL WITH MULTIPHASE CLOCKS

Field of the invention

[0001] The present invention is related to a fractional-N frequency synthesizer used in digital communication systems. More precisely, it relates to a frequency synthesizer based on a Phase-Locked Loop (PLL) with multiphase clocks, in which a self-calibrating loop is used.

State of the art

[0002] In many applications, e.g. in mobile radio systems, it is necessary to synthesize frequencies in a digital way, i.e. using a Phase-Locked Loop. A conventional integer-N frequency synthesizer produces an output frequency that is N times the input reference frequency, such that its frequency resolution is the same as the PLL reference frequency. Therefore, narrow channel spacing is accompanied by a small loop bandwidth, which leads to long settling times. With a fractional-N frequency synthesizer an output frequency is generated that is N+X/Y times the input reference frequency, i.e. a fractional multiple of the reference frequency, such that narrow channel spacing is achieved along with a higher phase detector frequency. If Y is not too big the fractional-N frequency synthesizer can be based on multiphase clock signals. The Voltage Controlled Oscillator (VCO) then disposes of Y copies of

the signal, each shifted over $2\pi/Y$. The value of X then determines at which instances a VCO output pulse is generated.

[0003] Several major drawbacks arise from this approach. A mismatch between the various clock signal phases causes reduced quadrature accuracy, if the phases are used in an image-reject transceiver. Further, when the PLL is locked, the delay mismatches introduce periodic phase errors that give rise to fractional spurs in the output frequency spectrum, resulting in an out-of-spec transmitter spectrum and in a reduced interference capability in the receiver. A solution to this problem is suggested in IEEE JSSC, Vol. 36, No.5, May 2001, pp.777-783. It consists in adding to the PLL a self-calibrating loop to eliminate the delay mismatches. The calibration loop adjusts the phases of the multiphase clock signal based on the timing information present in the phase frequency detector (PFD) outputs. The calibration loop has a much smaller bandwidth to avoid disturbance of the locking behaviour of the main loop. A safe solution here is to activate the calibration loop only when the main loop is locked. In the calibration loop there is a multiplexing switch that guides the current coming out of the calibration charge pump towards one of the Y calibration loop filters. Which one of the Y calibration loop filters is to be selected, is determined by a control logic that knows which phase is currently selected by the phase-switching fractional divider and thus knows which phase must be calibrated.

[0004] To adjust the phase of the multiphase clocks, extra circuitry must be inserted in the VCO or in the high-speed divide-by-2 prescalers. This inevitably slows down

Anmeldung Nr:
Application no.: 02447228.4
Demande no:

Anmeldetag:
Date of filing: 21.11.02
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

STMicroelectronics Belgium N.V.
Excelsiorlaan 44-46
1930 Zaventem
BELGIQUE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Low frequency self-calibration of a PLL with multiphase clocks

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H03L/

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR